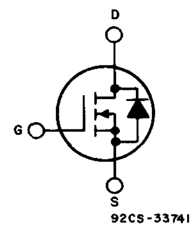
N-Channel Enhancement-Mode Power Field-Effect Transistors

11.5 A, 400 V
$r_{DS(on)} = 0.4\ \Omega$

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

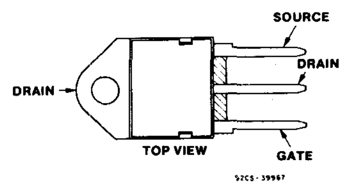


TERMINAL DIAGRAM

The BUZ 351 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ 351 is supplied in the JEDEC TO-218AC plastic package.

TERMINAL DESIGNATION



JEDEC TO-218AC

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

DRAIN-SOURCE VOLTAGE	V_{DSS}	400	V
DRAIN-GATE VOLTAGE, R_{DS} = 20 kΩ	V_{DGR}	400	V
GATE-SOURCE VOLTAGE	V_{GS}	±20	V
DRAIN CURRENT, RMS Continuous T_C = 30 °C	I_D	11.5	A
Pulsed T_C = 25 °C	I_{DM}	46	A
POWER DISSIPATION @ T_C = 25 °C	P_T	125	W
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150	°C
DIN HUMIDITY CATEGORY — DIN 40040		E	
IEC CLIMATIC CATEGORY — DIN IEC 68-1		55/150/56	

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0$ V $I_D = 0.25$ mA	400	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ $I_D = 1$ mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	$T_j = 25$ °C $T_j = 125$ °C $V_{DS} = 400$ V, $V_{GS} = 0$ V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 20$ V $V_{DS} = 0$ V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	$V_{GS} = 10$ V $I_D = 5.5$ A	—	0.35	0.4	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25$ V $I_D = 5.5$ A	3.3	4.5	—	S
Input Capacitance	C_{iss}	$V_{GS} = 0$ V $V_{DS} = 25$ V f = 1 MHz	—	3.8	4.9	nF
Output Capacitance	C_{oss}		—	300	500	pF
Reverse Transfer Capacitance	C_{rss}		—	120	200	pF
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	$V_{CC} = 30$ V $I_D = 2.9$ A $V_{GS} = 10$ V $R_{GS} = 50$ Ω	—	50	75	ns
	t_r		—	80	120	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$		—	330	430	ns
	t_f		—	110	140	ns
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 1			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 45			°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	$T_C = 25$ °C	—	—	11.5	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	46	A
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$ $V_{GS} = 0$ V, $T_j = 25$ °C	—	1.3	1.7	V
Reverse Recovery Time	t_{rr}	$T_j = 25$°C, $I_F = I_{DR}$ $dI_F/dt = 100$ A/μs, $V_R = 100$ V	—	1	—	ns
Reverse Recovered Charge	Q_{RR}		—	10	—	μC

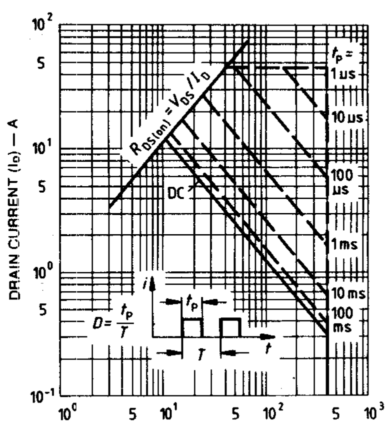


Fig. 1 - Maximum safe operating areas for all types.

BUZ 351

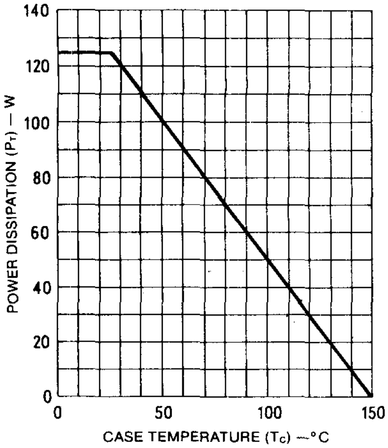


Fig. 2 - Power vs. temperature derating curve for all types.

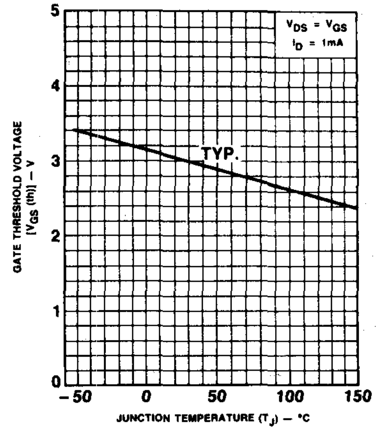


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

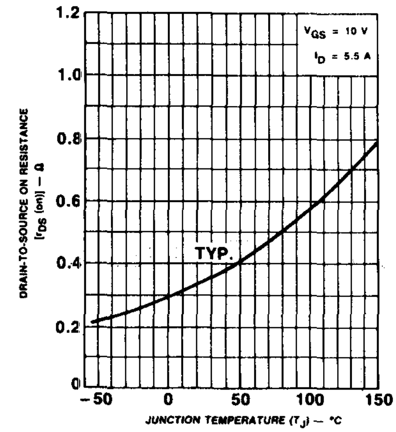


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

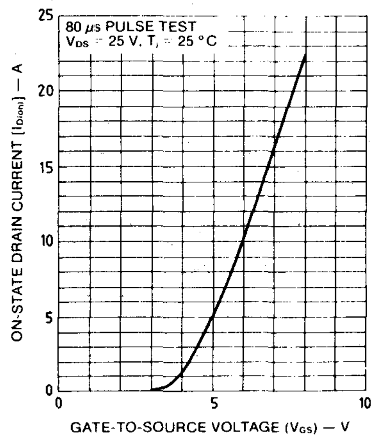


Fig. 5 - Typical transfer characteristics for all types.

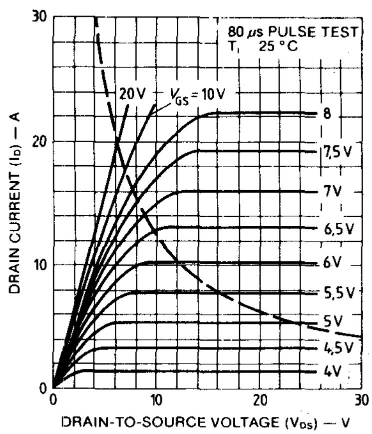


Fig. 6 - Typical output characteristics.

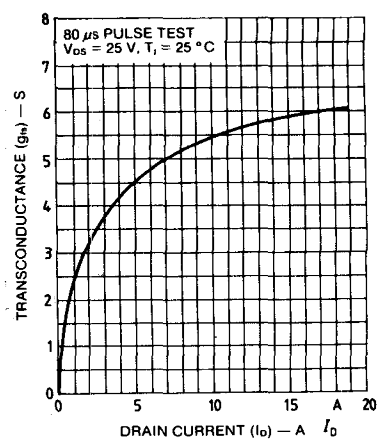


Fig. 7 - Typical transconductance vs. drain current.

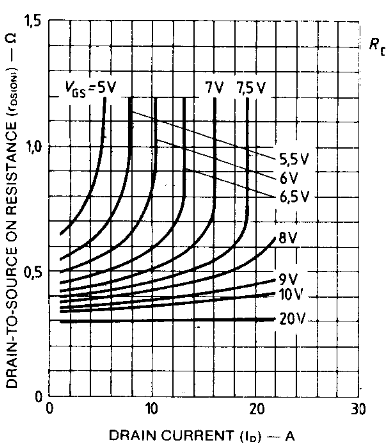


Fig. 8 - Typical on-resistance vs. drain current.

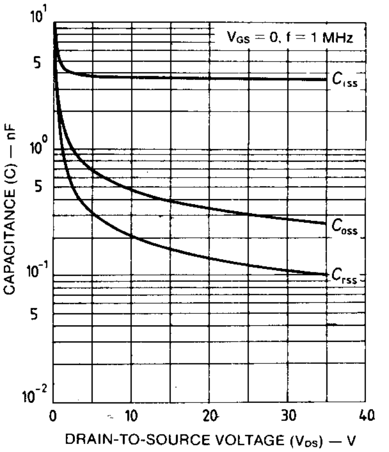


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

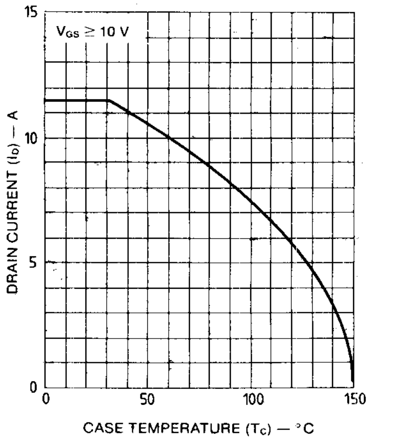


Fig. 10 - Maximum drain current vs. case temperature.

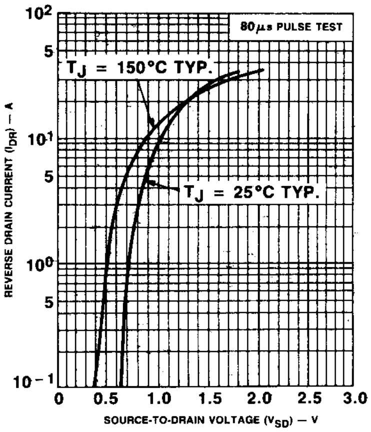


Fig. 11 - Typical source-drain diode forward voltage.

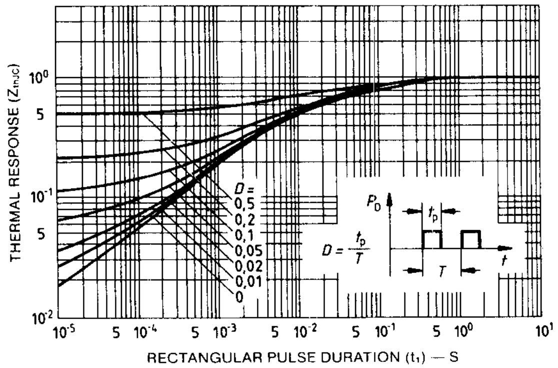


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

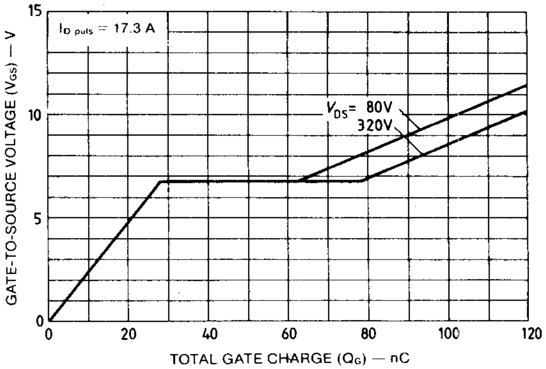


Fig. 13 - Typical gate charge vs. gate-to-source voltage.