

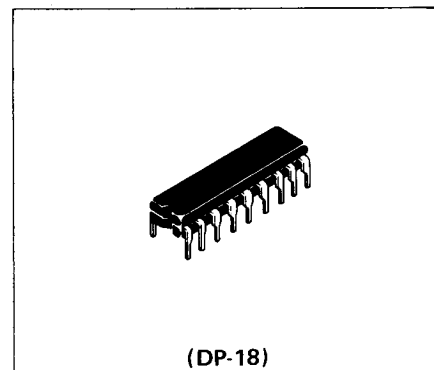
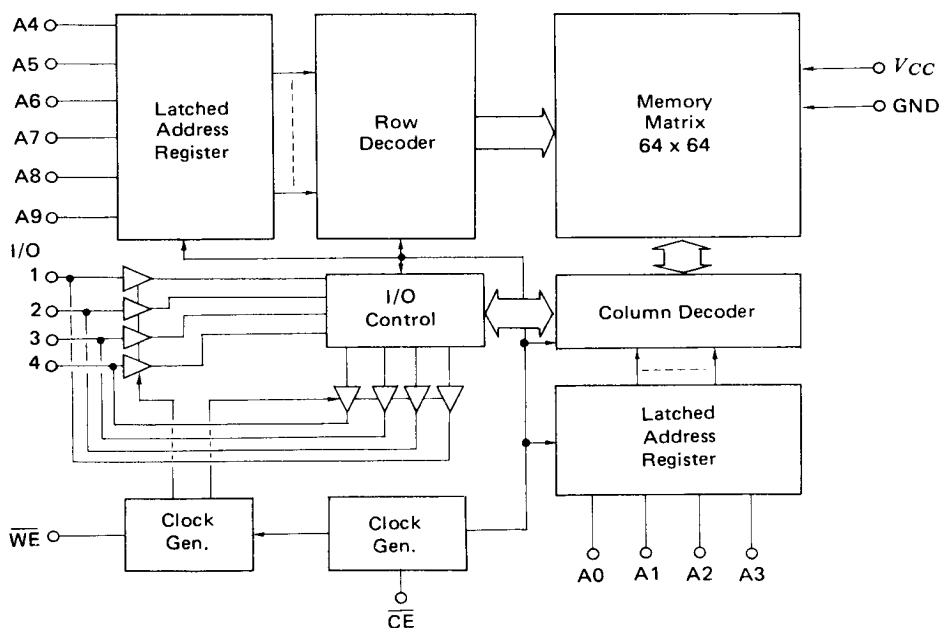
HM4334P-3, HM4334P-4

1024-word X 4-bit Static CMOS RAM

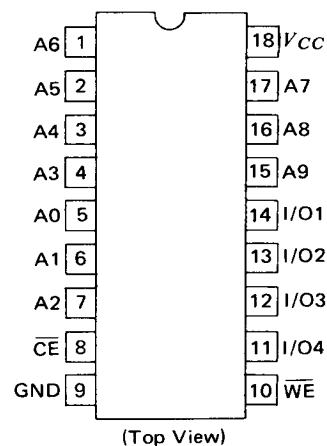
■ FEATURES

- Single 5V Supply
- Low Power Standby and Low Power Operation; Standby: 10 μ W (typ.)
Operation: 20 mW (typ.)
- Fast Access Time; HM4334P-3: 300 ns (max.)
HM4334P-4: 450 ns (max.)
- Directly TTL Compatible: All inputs and outputs
- Common Data Input and Output using Three-state Outputs
- On Chip Address Register

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage On Any Pin *	V_T	-0.3 to $V_{CC} + 0.5$	V
Power Supply Voltage *	V_{CC}	-0.3 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	$^{\circ}$ C
Storage Temperature	T_{stg}	-55 to +125	$^{\circ}$ C

* relative to GND

HM4334P-3, HM4334P-4

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	HM4334P-3			HM4334P-4			Unit
		min.	typ.	max.	min.	typ.	max.	
Supply Voltage	V_{CC}	4.75	5.0	5.25	4.5	5.0	5.5	V
	GND	0	0	0	0	0	0	V
Input Voltage	V_{IH}	2.4	—	$V_{CC} + 0.5$	2.4	—	$V_{CC} + 0.5$	V
	V_{IL}	-0.3	—	0.8	-0.3	—	0.8	V

■ DC AND OPERATING CHARACTERISTICS

($T_a = 0$ to $+70^\circ\text{C}$, GND = 0V, HM4334P-3: $V_{CC} = 5V \pm 5\%$, HM4334P-4: $V_{CC} = 5V \pm 10\%$)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	-1.0	—	+1.0	μA
Output Leakage Current	I_{LO}	$\overline{CE} = V_{IH}$, $V_{out} = 0$ to V_{CC}	-1.0	—	+1.0	μA
Operating Power Supply Current	I_{CC1}	$\overline{CE} = 0V$, $V_{IN} = V_{CC}$, $I_{I/O} = 0$	—	—	1.0	mA
	I_{CC2}	$\overline{CE} = 0.8V$, $V_{IN} = 2.4V$, $I_{I/O} = 0$	—	2.5	5.0	mA
Average Operating Current	I_{CC3}	$V_{IN} = 0$ or V_{CC} , $f = 1\text{MHz}$, duty 50%, $I_{I/O} = 0$	—	4	7	mA
Standby Power Supply Current	I_{CCL}	$\overline{CE} \geq V_{CC} - 0.2V$	—	2	100	μA
Output Voltage	V_{OL}	$I_{OL} = 2.0\text{mA}$	—	—	0.4	V
	V_{OH}	$I_{OH} = -1.0\text{mA}$	2.4	—	—	V

■ CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
I/O Terminal Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	7	10	pF
Input Capacitance	C_{in}	$V_{in} = 0V$	—	3	5	pF

■ AC CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$, GND = 0V, HM4334P-3: $V_{CC} = 5V \pm 5\%$, HM4334P-4: $V_{CC} = 5V \pm 10\%$)

Item	Symbol	HM4334P-3			HM4334P-4			Unit
		min.	typ.	max.	min.	typ.	max.	
Read or Write Cycle Time *	TELEL t_C	460	—	—	640	—	—	ns
Chip Enable Access Time	TELQV t_{AC}	—	—	300	—	—	450	ns
Chip Enable to Output Active	TELQX t_{CX}	50	—	—	50	—	—	ns
Output 3-state from Deselection	TEHQZ t_{OFF1}	—	—	100	—	—	100	ns
Write Enable Output Disable Time	TWLQZ t_{OFF2}	—	—	100	—	—	100	ns
Chip Enable Pulse Width **	TELEH t_{CE}	300	—	—	450	—	—	ns
Chip Enable Precharge Time	TEHEL t_p	120	—	—	150	—	—	ns
Address Hold Time	TELAX t_{AH}	100	—	—	100	—	—	ns
Address Setup Time	TAVEL t_{AS}	20	—	—	20	—	—	ns
Read Setup Time	TWHEL t_{RS}	0	—	—	0	—	—	ns
Read Hold Time	TEHWL t_{RH}	0	—	—	0	—	—	ns
Write Enable Setup Time	TWLEL t_{WS}	-20	—	—	-20	—	—	ns
\overline{WE} to \overline{CE} Precharge Lead Time	TWLEH t_{WPL}	300	—	—	450	—	—	ns
Chip Enable to Write Enable Delay Time	TELWL t_{CWD}	300	—	—	450	—	—	ns
Write Enable Hold Time	TEHWH t_{EWH}	0	—	—	0	—	—	ns
Write Hold Time	TELWH t_{WH}	300	—	—	450	—	—	ns
Data Input Setup Time	TDVWH TDVEH t_{DS}	200	—	—	350	—	—	ns
Data Hold Time	TWHDX TEHDX t_{DH}	0	—	—	0	—	—	ns
Write Data Delay Time	TWLDV t_{WDS}	100	—	—	100	—	—	ns
Chip Enable Rise/Fall Time	TT t_T	—	—	300	—	—	300	ns

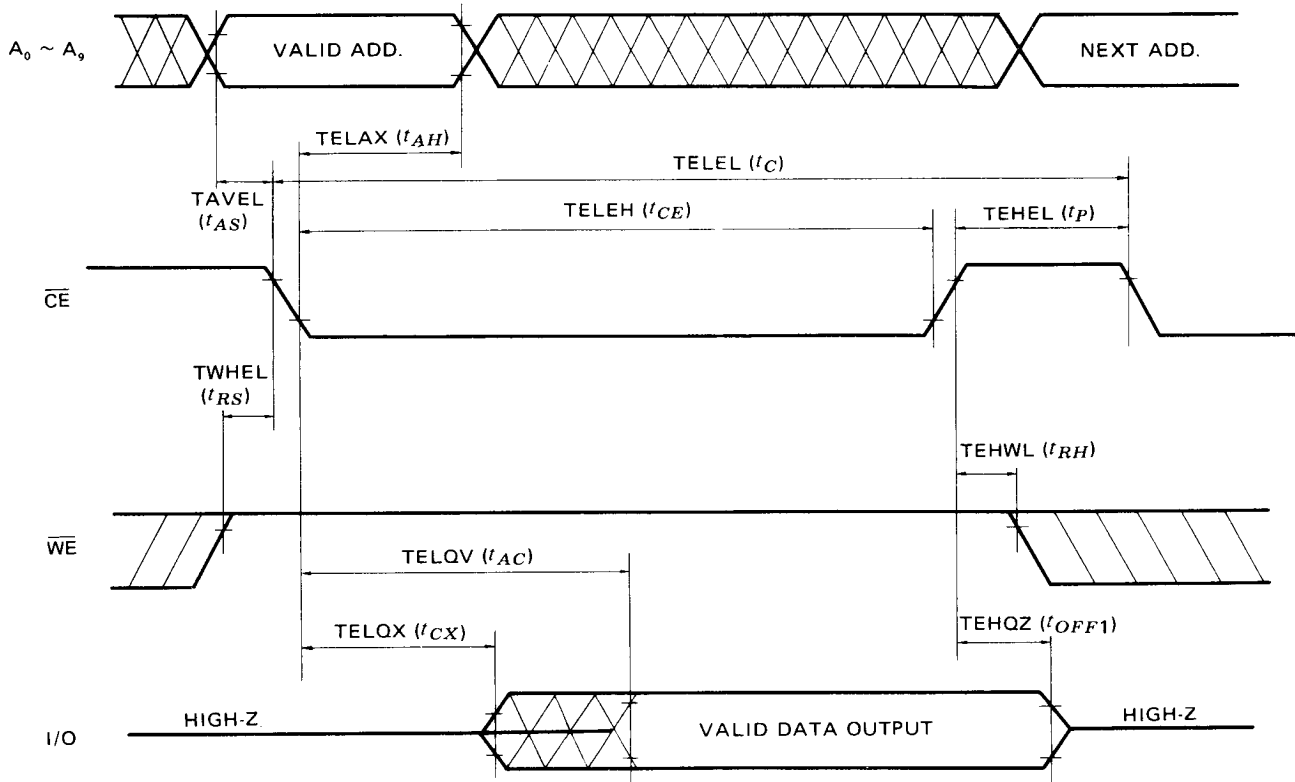
* TELEL (t_C) = TELEH (t_{CE}) + TEHEL (t_p) + t_r (20ns) + t_f (20ns)

** For Read Modify Write Cycle, TELEH (t_{CE}) = TELWL (t_{CWD}) + TWLEH (t_{WPL}) + t_f (20ns)

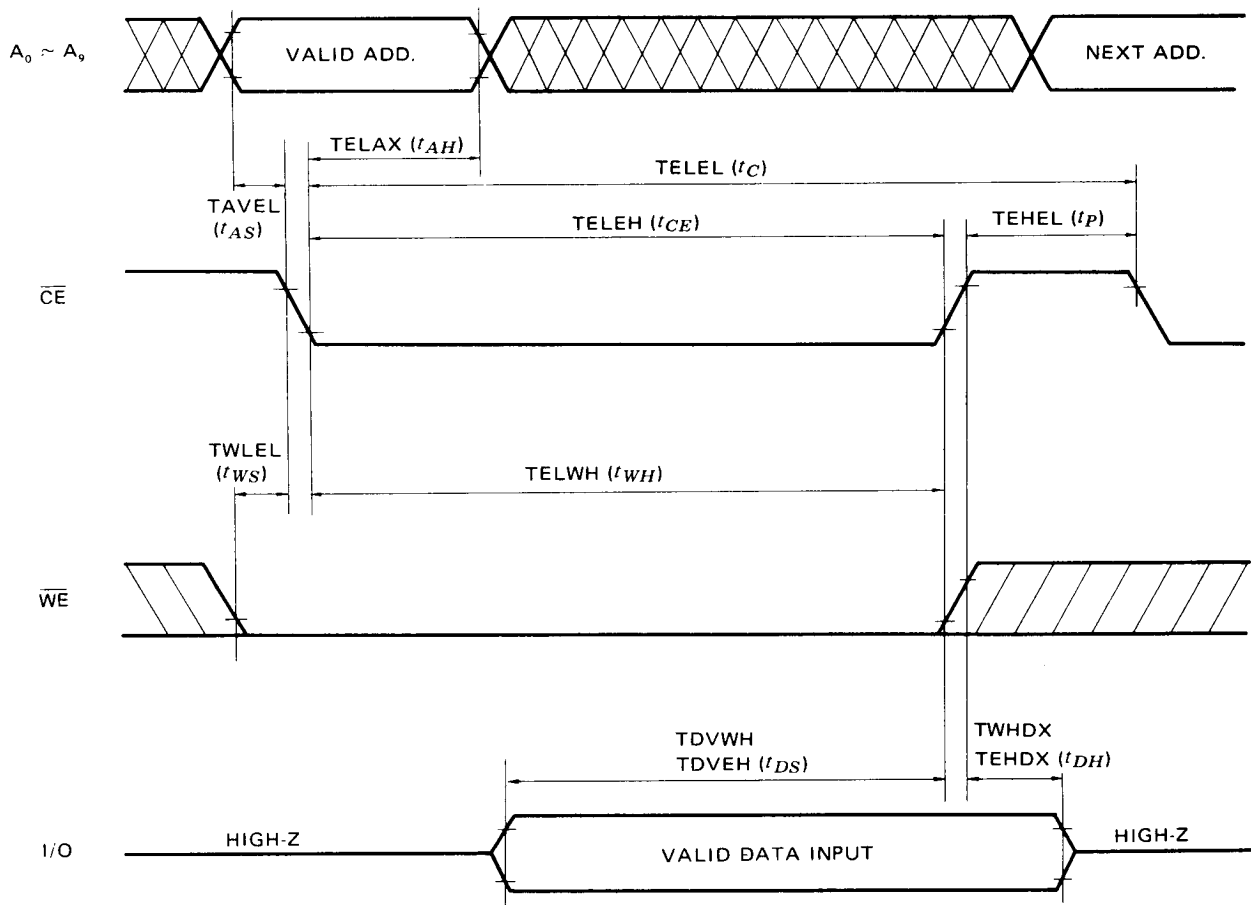
■ AC TEST CONDITIONS

Input Level 2.4V, 0.8V
 Input Rise and Fall Time 20 ns
 Timing Measurement Level 2.4V, 0.8V
 Reference Level $V_{OH} = 2.0V, V_{OL} = 0.8V$
 Output Load 1 TTL and $C_L = 100\text{ pF}$

● READ CYCLE

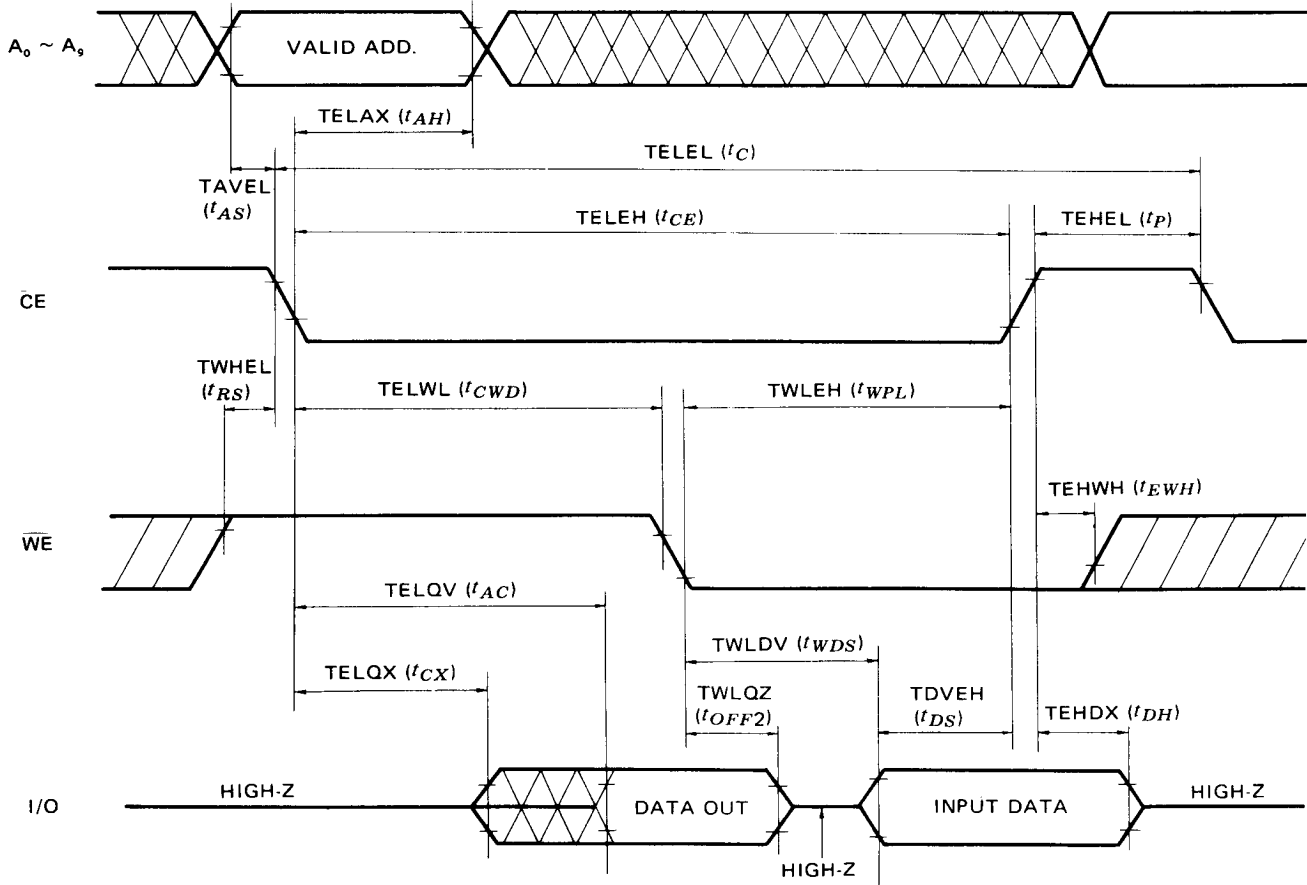


• WRITE CYCLE

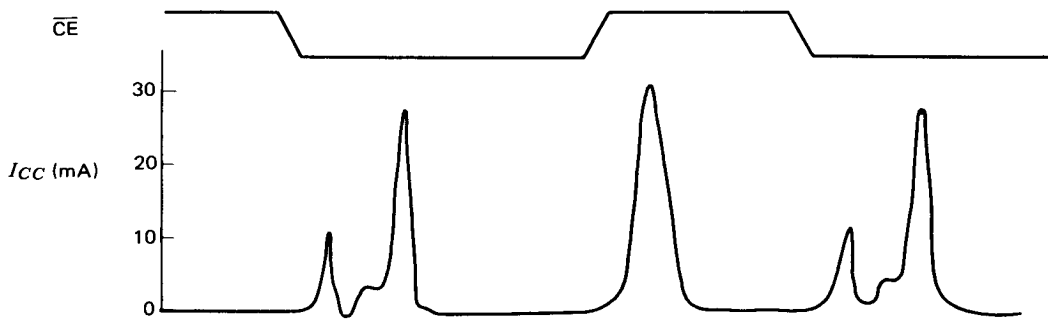


NOTE: t_{DS} and t_{DH} are measured from the earlier of \overline{CE} or \overline{WE} going high.

• READ MODIFY WRITE CYCLE



• CURRENT WAVEFORM



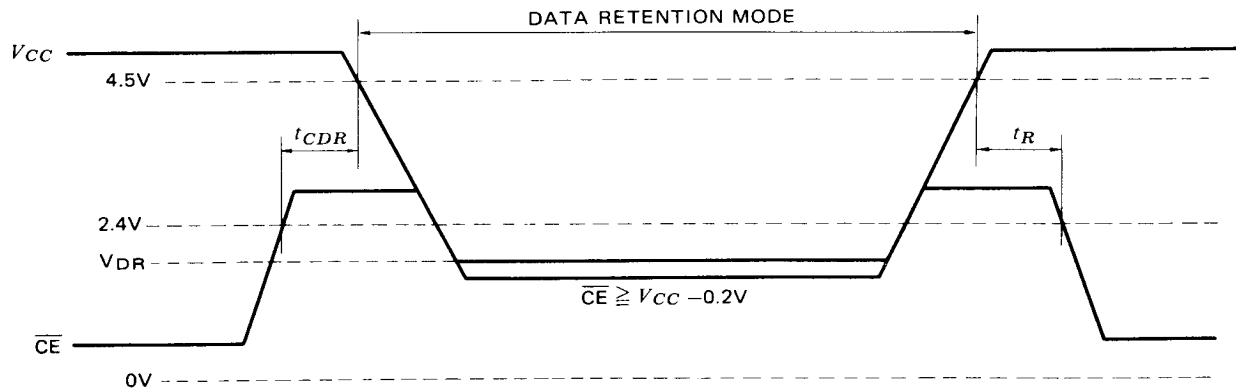
[NOTE] $V_{CC} = 5.0V, T_a = 25^\circ C$

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$)

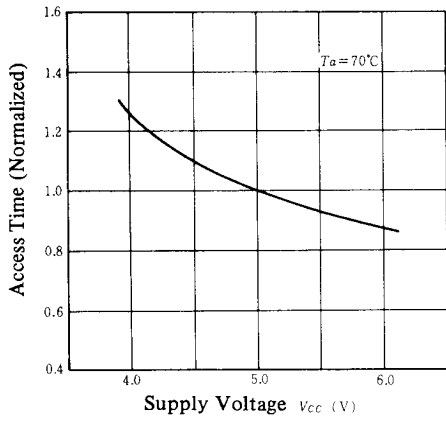
Item	Symbol	Test Condition	min.	typ.	max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CE} \geq V_{CC} - 0.2V$	2.0	—	—	V
Data Retention Power Supply Current	I_{CCDR}	$V_{DR} = 3.0V$	—	0.5	50	μA
Chip Deselection to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC}^*	—	—	ns

* t_{RC} = Read Cycle Time

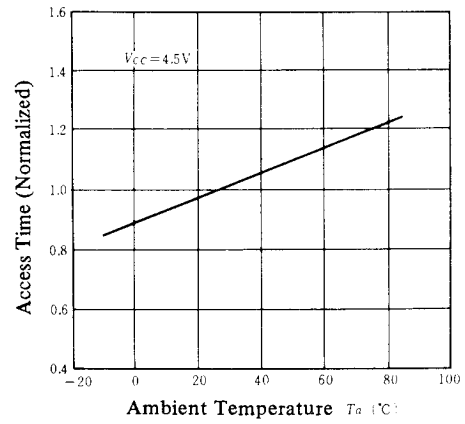
● LOW V_{CC} DATA RETENTION TIMING



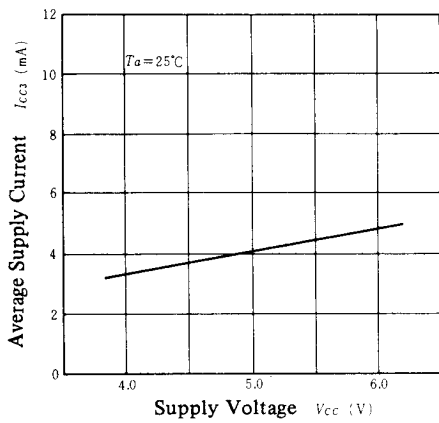
ACCESS TIME vs. SUPPLY VOLTAGE



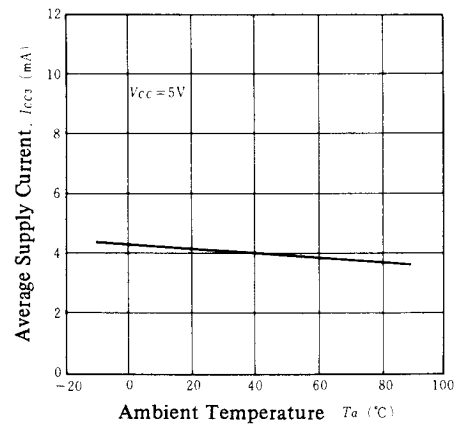
ACCESS TIME vs. AMBIENT TEMPERATURE



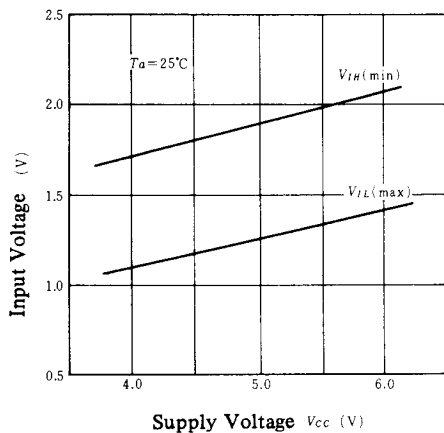
AVERAGE SUPPLY CURRENT vs. SUPPLY VOLTAGE



AVERAGE SUPPLY CURRENT vs. AMBIENT TEMPERATURE



INPUT VOLTAGE vs. SUPPLY VOLTAGE



INPUT VOLTAGE vs. AMBIENT TEMPERATURE

