

MOS  
LSI

TMS 4027 JL, NL  
4096-BIT DYNAMIC RANDOM-ACCESS MEMORY

DRAWING

- 4096 X 1 Organization
- Industry Standard 16-Pin 300-Mil Package Configuration
- 10% Tolerance on All Supplies
- All Inputs Including Clocks TTL Compatible
- Three-State Fully TTL-Compatible Output Latched and Valid Into Next Cycle

3 Performance Ranges:

	ACCESS TIME	ACCESS TIME	READ OR WRITE CYCLE	READ, MODIFY-WRITE† CYCLE
	(MAX)	(MAX)	(MIN)	(MIN)
TMS 4027-15	150 ns	100 ns	320 ns	330 ns
TMS 4027-20	200 ns	135 ns	375 ns	420 ns
TMS 4027-25	250 ns	165 ns	375 ns	480 ns

- Page-Mode Operation for Faster Access Time
- Low-Power Dissipation
  - Operating 460 mW (max)
  - Standby 27 mW (max)
- 1-T Cell Design, N-Channel Silicon-Gate Technology

Description

The TMS 4027 JL, NL series is composed of monolithic high-speed dynamic 4096-bit MOS random-access memories, organized as 4096 one-bit words, employing single-transistor storage cells and N-channel silicon-gate technology.

All inputs and outputs are compatible with Series 74 TTL circuits including clocks: Row Address Strobe (RAS) or (R) and Column Address Strobe (CAS) or (C). All address lines (A0 through A5) and data-in (D) are latched on chip to simplify system design. Data out is latched and available until the negative edge of CAS in the next memory cycle returns the output to the high-impedance state.

Typical power dissipation is less than 300 milliwatts active and 14 milliwatts during standby (VCC is not required during standby operation). To retain data, only 20 milliwatts average power is required which includes the power consumed to refresh the contents of the memory.

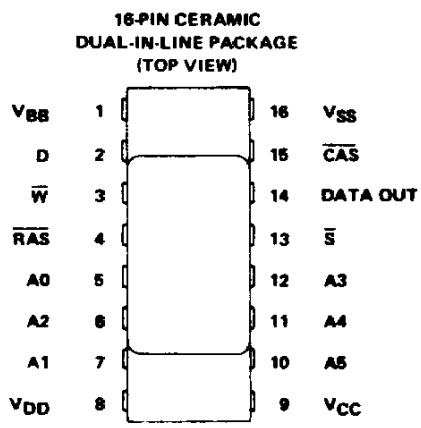
The TMS 4027 JL, NL series is offered in a 16-pin dual-in-line package and is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting-hole rows on 300-mil centers.

Operation

address (A0 through A5)

Twelve address bits are required to decode 1 of 4096 storage cell locations. Six row-address bits are set up on pins A0 through A5 and latched onto the chip by the row-address strobe (RAS). Then the six column-address bits are set up on

† The term "read-write cycle" is sometimes used as an alternative title to "read-modify-write cycle".



PIN NAMES

A0-A5	Address Inputs
CAS	Column address strobe
D	Data input
DATA OUT	Data output
RAS	Row address strobe
S	Chip select
W	Write enable
VBB	-5 V power supply
VCC	+5 V power supply
VDD	+12 V power supply
VSS	0 V ground

PRELIMINARY DATA SHEET: supplementary data will be published at a later date.

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pins A0 through A5 and latched onto the chip by the column-address strobe ( $\overline{\text{CAS}}$ ).  $\overline{\text{RAS}}$  activates the sense amplifiers as well as the row decoder, and  $\overline{\text{CAS}}$  activates the column decoder and the input and output buffers.

#### chip select ( $\overline{\text{S}}$ )

When the chip select ( $\overline{\text{S}}$ ) input is high, the column decode and the input and output buffers are disabled. However, the row decode is unaffected by chip select so that row addresses are latched and refresh can continue to take place.

#### write enable ( $\overline{\text{W}}$ )

The read or write mode is selected through the write enable ( $\overline{\text{W}}$ ) input. A logic high on the  $\overline{\text{W}}$  input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When  $\overline{\text{W}}$  goes low prior to  $\overline{\text{CAS}}$  (early write), data-out will contain the data written into the selected cell.

#### data-in (D)

Data is written during a write or read modify-write cycle. The latter falling edge of  $\overline{\text{CAS}}$  or  $\overline{\text{W}}$  strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle  $\overline{\text{W}}$  is brought low prior to  $\overline{\text{CAS}}$  and the data is strobed in by  $\overline{\text{CAS}}$  with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle,  $\overline{\text{CAS}}$  will already be low, thus the data will be strobed in by  $\overline{\text{W}}$  with setup and hold times referenced to this signal.

#### data-out

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output goes into the high-impedance state after the negative transition of  $\overline{\text{CAS}}$ . The output becomes valid after the access time has elapsed, and it remains valid into the next memory cycle before  $\overline{\text{CAS}}$  going low returns it to a high-impedance state.

#### refresh

A refresh operation must be performed at least every two milliseconds to retain data. Since the output buffer is in the high-impedance state unless  $\overline{\text{CAS}}$  is applied, the  $\overline{\text{RAS}}$  only refresh sequence avoids any output during refresh. Strobing each of the 64 row addresses (A0 through A5) with  $\overline{\text{RAS}}$  causes all bits in each row to be refreshed.  $\overline{\text{CAS}}$  remains high (inactive) for this refresh sequence, thus conserving power.

#### page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe the row addresses is eliminated. To extend beyond the 64 column locations on a single RAM, apply the row address and  $\overline{\text{RAS}}$  to multiple 4K RAMs, then decode chip select to select the proper RAM. (A RAM need not be selected during the first page mode cycles to have the row address latched on chip.)

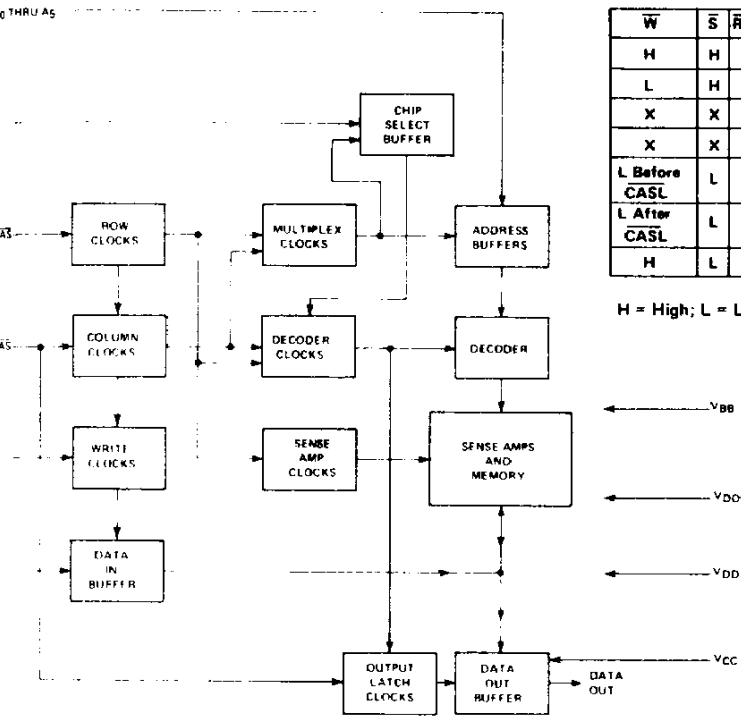
#### power up

$V_{\text{BB}}$  must be applied to the device either before or at the same time as the other supplies and removed last. Failure to observe this precaution will cause dissipation in excess of the absolute maximum ratings due to internal forward bias conditions. This also applied to system use where failure of the  $V_{\text{BB}}$  supply must immediately shut down the other supplies. After power up, eight memory cycles must be performed to achieve proper device operation.

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Functional block diagram



W	S	RAS	CAS	OUTPUT	MODE
H	H	L	L	Hi-Z	Not selected
L	H	L	L	Hi-Z	No write will occur
X	X	L	H	Hi-Z	RAS only cycle
X	X	H	L	Hi-Z	CAS only cycle
L Before CASL	L	L	L	Input data	Early write
L After CASL	L	L	L	Valid data	Write or read/write cycle
H	L	L	L	Data out	Read

H = High; L = Low; X = Don't Care; Hi-Z = High impedance.

DRAWN

**Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)\***

Supply voltage, VCC (see Note 1)	-0.3 to 20 V
Voltage on VDD, VCC, relative to VSS	-1.0 to 15 V
Supply voltage, VDD (see Note 1)	-0.3 to 20 V
Supply voltage, VSS (see Note 1)	-0.3 to 20 V
All input voltages (see Note 1)	-0.3 to 20 V
Output voltage (operating, with respect to VSS)	-2 to 10 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, VBB (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to VSS.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and not a recommended operating condition. Operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**Recommended operating conditions**

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, VBB	-4.5	-5	-5.5	V
Supply voltage, VCC	4.5	5	5.5	V
Supply voltage, VDD	10.8	12	13.2	V
Supply voltage, VSS		0		V
High-level input voltage, except RAS, CAS, and WRITE, VIH	2.2	3.5	7	V
High-level input voltage, RAS, CAS, and WRITE, VIH(R)	2.4	3.5	7	V
Low-level input voltage, VIL	-1	0	0.8	V
Refresh time, trefresh			2	ms
Operating free-air temperature, TA	0		70	°C

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -5 mA	2.4			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 3.2 mA, C <sub>L</sub> = 50 pF			0.4	V
I <sub>I</sub>	Input current (leakage)	V <sub>I</sub> = 0 V to 10 V, All other pins = 0 V except V <sub>BB</sub> = -5 V			10	μA
I <sub>O</sub>	Output current (leakage)	V <sub>O</sub> = 0 to 10 V, RAS and CAS high, Output disabled, after 1 memory cycle			10	μA
I <sub>BB(av)</sub>	Average operating current during read or write cycle	Minimum cycle time		90	150	μA
I <sub>CC(av)*</sub>						
I <sub>DD(av)</sub>		Minimum cycle time		25	35	mA
I <sub>OD</sub>	Standby current, RAS, CAS, and CS high	Chip deselected after 1 memory cycle		0.85	2	mA
	RAS, CAS high, CS low			2	4	
I <sub>DD(av)</sub>	Average refresh current, RAS cycling, CAS high	Minimum cycle time		15	25	mA
I <sub>BB</sub>	Standby current, RAS, CAS, CS high			90	150	μA

\*V<sub>CC</sub> is applied only to the output buffer, so I<sub>CC</sub> depends on output loading.

capacitance over recommended supply voltage range and operating free-air temperature range f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
C <sub>i(A)</sub>	Input capacitance, address inputs	4	5	pF
C <sub>i(D)</sub>	Input capacitance, data input	4	5	pF
C <sub>i(RC)</sub>	Input capacitance, strobe inputs	8	10	pF
C <sub>i(W)</sub>	Input capacitance, write enable input	8	10	pF
C <sub>o</sub>	Output capacitance	5	7	pF

† All typical values are at T<sub>A</sub> = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER	TEST CONDITIONS	TMS 4027-15		TMS 4027-20		TMS 4027-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>a(C)</sub>	Access time from column address strobe C <sub>L</sub> = 50 pF, t <sub>r(C)</sub> and t <sub>r(R)</sub> = 5 ns.		100		135		165	ns
t <sub>a(R)</sub>	Access time from row address strobe †RL, CL = MAX, Load = 2 Series 74 TTL gates		150		200		250	ns
tpvZ	Output valid time C <sub>L</sub> = 50 pF,	10		10		10		μs
tpxZ	Output disable time Load = 2 Series 74 TTL gates	0	40	0	50	0	60	ns

## TMS 4027 JL, NL 4096-BIT DYNAMIC RANDOM-ACCESS MEMORY

Timing requirements over recommended supply voltage range and operating free-air temperature range

DRAMs

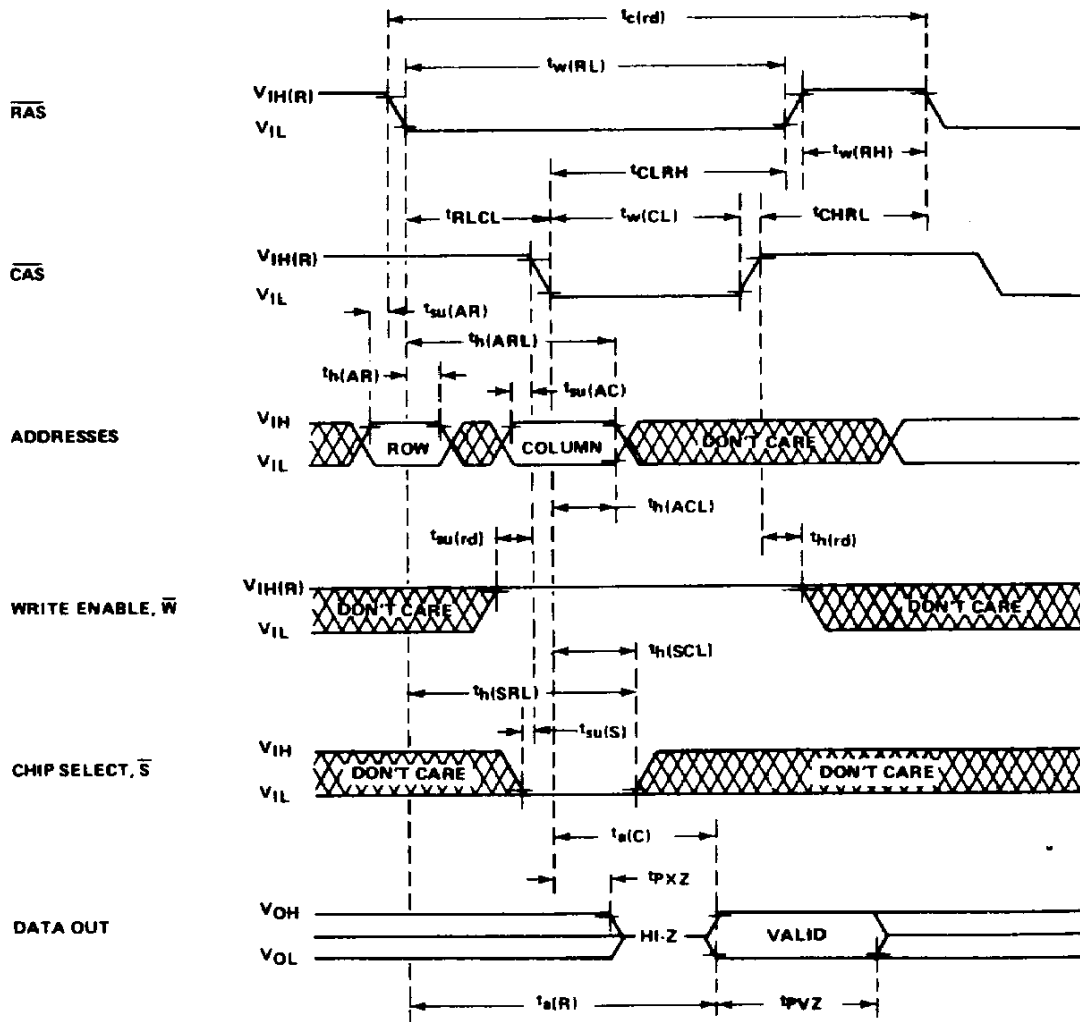
PARAMETER	TMS 4027-15		TMS 4027-20		TMS 4027-25		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>rd</sub> Read cycle time	320		375		375		ns
t <sub>w</sub> Write cycle time	320		375		375		ns
t <sub>RW</sub> Read, modify-write cycle time	330		420		480		ns
t <sub>CH</sub> Pulse width, column address strobe high (precharge time)	60		80		110		ns
t <sub>CL</sub> Pulse width, column address strobe low	100		135		165		ns
t <sub>RH</sub> Pulse width, row address strobe high (precharge time)	100		120		120		ns
t <sub>RL</sub> Pulse width, row address strobe low	150	10,000	200	10,000	250	10,000	ns
t <sub>w</sub> Write pulse width	45		55		75		ns
Transition times (rise and fall) for RAS and CAS	3	35	3	50	3	50	ns
t <sub>AC</sub> Column address setup time	-10		-10		-10		ns
t <sub>AR</sub> Row address setup time	0		0		0		ns
t <sub>D</sub> Data setup time	0		0		0		ns
t <sub>CS</sub> Chip select setup time	-10		-10		-10		ns
t <sub>rd</sub> Read command setup time	0		0		0		ns
t <sub>WCH</sub> Write command setup time before CAS high	50		70		85		ns
t <sub>WRH</sub> Write command setup time before RAS high	50		70		85		ns
t <sub>ACL</sub> Column address hold time after CAS low	45		55		75		ns
t <sub>AR</sub> Row address hold time	20		25		35		ns
t <sub>ARL</sub> Column address hold time after RAS low	95		120		160		ns
t <sub>DCL</sub> Data hold time after CAS low	45		55		75		ns
t <sub>DRL</sub> Data hold time after RAS low	95		120		160		ns
t <sub>DWL</sub> Data hold time after W low	45		55		75		ns
t <sub>rd</sub> Read command hold time	0		0		0		ns
t <sub>SCL</sub> Chip select hold time after CAS low	45		55		75		ns
t <sub>SRL</sub> Chip select hold time after RAS low	95		120		160		ns
t <sub>WCL</sub> Write command hold time after CAS low	45		55		75		ns
t <sub>ARL</sub> Delay time, column address strobe high to row address strobe low	0		0		0		ns
t <sub>ARH</sub> Delay time, column address strobe low to row address strobe high	100		135		165		ns
t <sub>AWL</sub> Delay time, column address strobe low to W low (read, modify-write cycle only)	60		80		90		ns
t <sub>RF</sub> Refresh period		2		2		2	ms
t <sub>ACL</sub> Delay time, row address strobe low to column address strobe low (maximum value specified only to guarantee access time)	20	50	25	65	35	85	ns
t <sub>AWL</sub> Delay time, row address strobe low to W low (read, modify-write cycle only)	110		145		175		ns
t <sub>AWL</sub> Delay time, W low to column address strobe low (early write cycle)	0		0		0		ns

Note: All timing is measured from V<sub>IH(R)</sub> or V<sub>IH</sub> minimum and V<sub>IL</sub> maximum; V<sub>OH</sub> minimum and V<sub>OL</sub> maximum.

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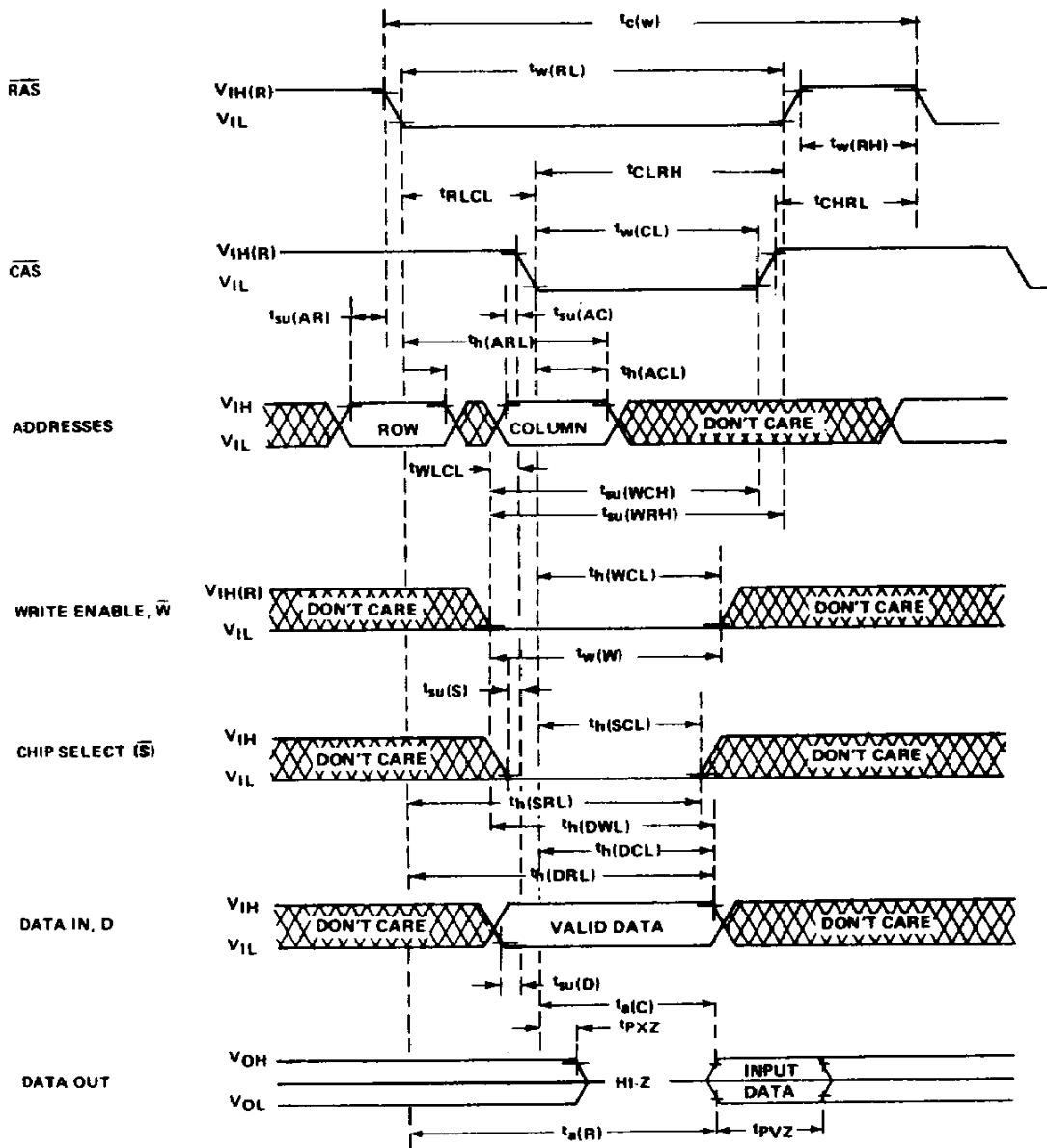
### read cycle timing



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## 4096-BIT DYNAMIC RANDOM-ACCESS MEMORY

early write cycle timing

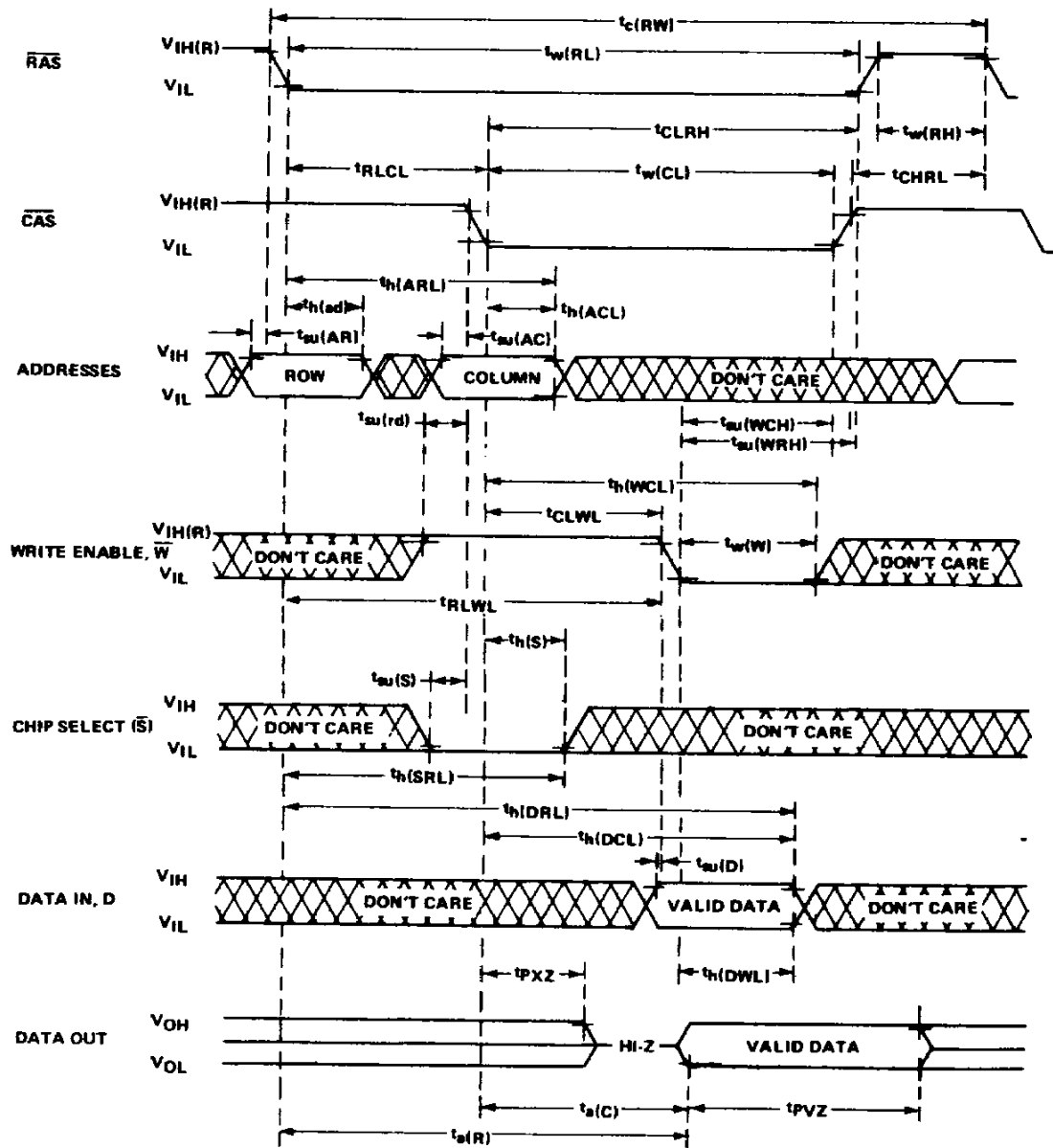


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## 4096-BIT DYNAMIC RANDOM-ACCESS MEMORY

read-write/read-modify-write cycle timing

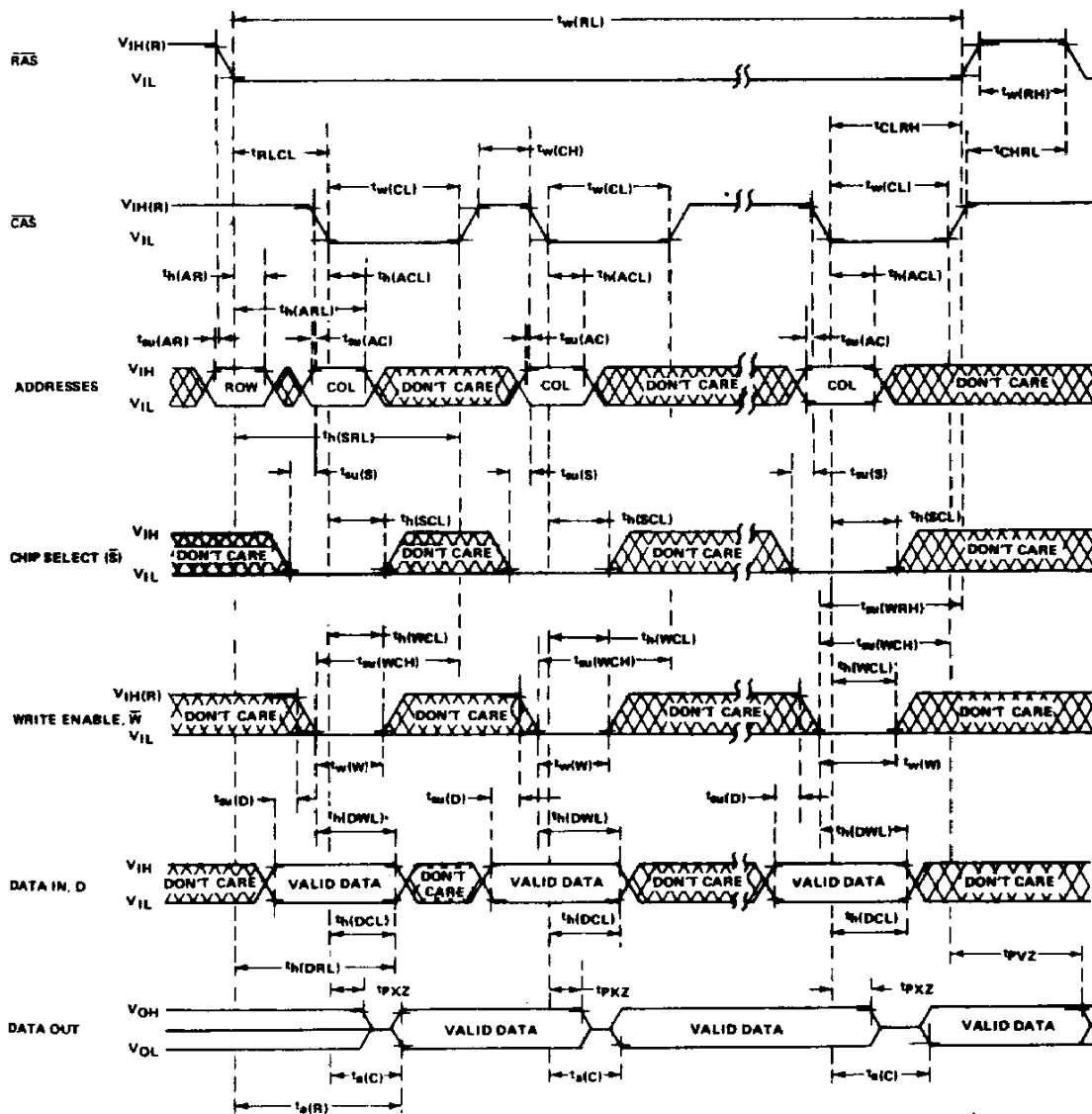




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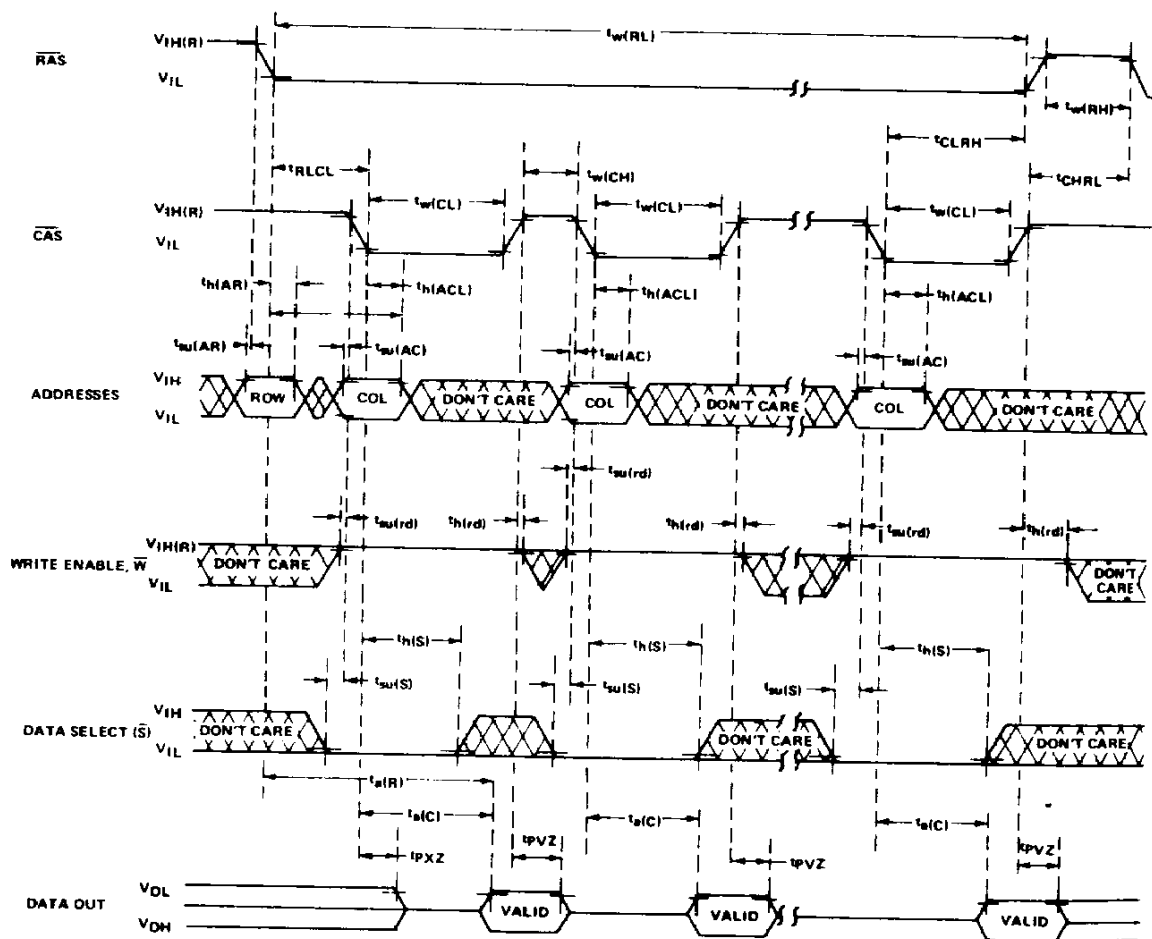
page mode write cycle timing



# TMS 4027 JL, NL

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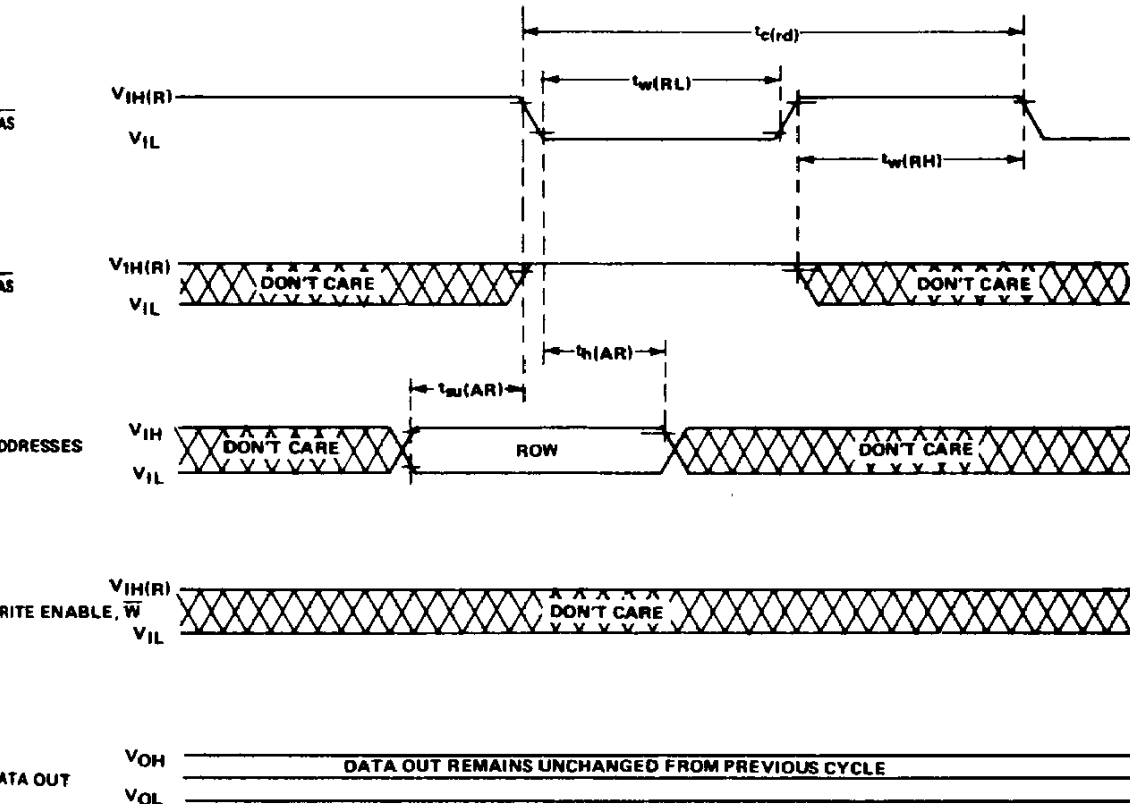
page mode read cycle timing



# TMS 4027 JL, NL 4096-BIT DYNAMIC RANDOM-ACCESS MEMORY

DRAMS

## AS only refresh timing



## Timing diagram conventions

TIMING DIAGRAM SYMBOL	MEANING	
	INPUT FORCING FUNCTIONS	OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't Care	State unknown or changing
	(Does not apply)	Center line is high-impedance off-state

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